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Ultra Thin Depleted Silicon On Insulator MOSFET: a simulation based on COMSOL Multiphysics

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Abstract

We use the MOS transistor model from COMSOL [1] as a template to develop our own UT-FD-SOI-MOSFET with an ultra thin geometry(Channel thickness = 10nm). SOI-MOSFETs are used to reduce short channel effect problems in actual MOSFET structures and to enable further miniaturization. Our model shows a linear dependence of the front Threshold Voltage with the Back Gate Voltage, which has been reported experimentally by [2] and theoretically by [3].

Keywords. UT-FD-SOI-MOSFET, Modeling, COMSOL Multiphysics, Threshold Voltage.

Resumen

Usamos el modelo de un transistor MOS de COMSOL [4] para desarrollar un nuevo modelo de un SOI-MOSFET completamente agotado y ulta delgado (profundidad de canal de 10nm). Los dispositivos MOSFET de Silicio en Aislante (Silicon On Insulator SOI-MOSFET) son utilizados para reducir los efectos de canal corto en estructuras MOSFET y lograr nuevos umbrales de miniaturización de los transistores. Nuestro modelo muestra una dependencia lineal del voltaje de umbral frontal con respecto al voltaje de compuerta posterior. Resultados similares se han reportado experimentalmente por [4] y teóricamente por [5].

Palabras Clave. SOI-MOSFET, Modelado Computacional, COMSOL Multiphysics, Voltaje de Umbral.

Introduction

MOSFET devices are the heart of modern microelectronics. The scaling of MOSFET transistor has followed Moore's law during the past 40 years [4], that is, the number of transistors per chip is increased at a rate of a factor of two every two years. However difficulties in transistor scaling caused the semiconductor community to slow down the miniaturization rate [5]. The main problem MOSFETs have when their size is very small is the presence of Short Channel Effects (SCE). We will consider two short channel phenomena: 1)Threshold Voltage is not constant with the channel length (Threshold Voltage Roll-Off) and 2)drain voltage causes a barrier lowering on the gate (Drain Induced Barrier Lowering or DIBL). To understand the Threshold Voltage Roll-Off we can imagine a long channel device and as the channel leght is reduced, the potential in the channel is also reduced due to the diffusion of the junction, hence less voltage is needed to produce an inversion layer [6]. The second effect is DIBL, in small devices, the fields produced by the gate add up to the field produced by the drain: the drain voltage influences the charge on the oxide-silicon interface.The DIBL is a degradation of the channel potential due to the drain bias. As a result of these effects, the current grows and the transistor consumes too much power in the off-state. If the off-state current increases and aproaches the on-state current, the two states are difficult to distinguish and control over the device is lost. It is desirable to have a mechanism that controls the threshold voltage. A possible solution to this problem is given by the Silicon On Insulator (SOI) technology. A back gate is introduced into the architecture of the device as can be seen in Figure 1, and the threshold voltage can be controlled by the Back Gate Voltage V_{GB}.

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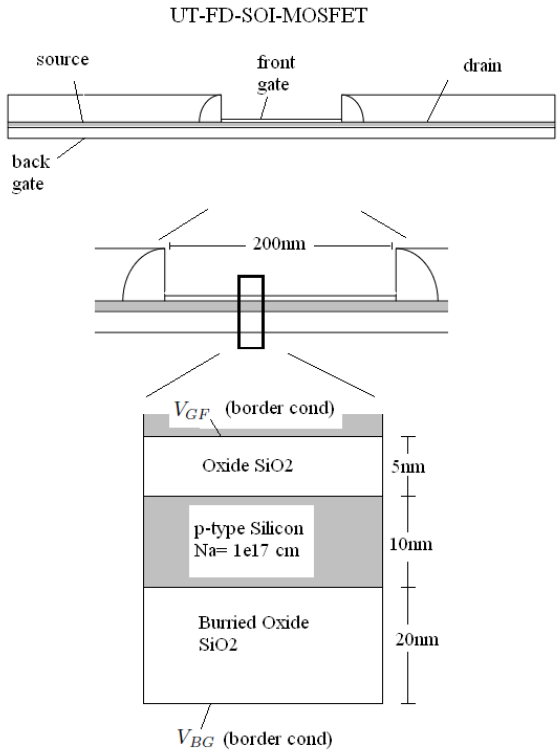

Figure 1: Device architecture. The broad picture of the geometry is described. In the gate there is a front oxide, a Silicon channel, and a back oxide. The front and back gate voltages are boundary conditions, and the polysilicon is not simulated.

We model the device using the equation of Poisson, coupled with the equations of diffusion and convection of electrons and holes. The model produces, in addition to qualitative phenomena as the creation of a channel, the intended Current-Voltage characteristics of a SOI-MOSFET and a linear dependence of V_{th} with V_{GB}. Throughout this work we will consider a n-channel device.

Methods

We define a system of differential equations which will be solved simultaneously. We solve Poisson's equation for the potential on the transistor ψ, the concentration of electrons *n* and the concentration of holes *p*. The initial guess of the simulation will be calculated from a Doping function which defines the doping on the n-type source and drain regions to $N_d = 1 \times 10^{19} cm^{-3}$, the doping on the substrate to $N_a = 5 \times 10^{17} cm^{-3}$. The transition between the regions is Gaussian. Then, the following equations are solved iteratively to find the ψ, n, p. Poisson's Equation,

$$\nabla \cdot (\epsilon \nabla \psi_p) = -q\,(p - n - N_a) \tag{1}$$

Drift and diffusion equations

$$J_p = -qp\mu_p \nabla\psi - qD_p \nabla p \tag{2}$$

$$J_n = -qn\mu_n \nabla\psi - qD_n \nabla n \tag{3}$$

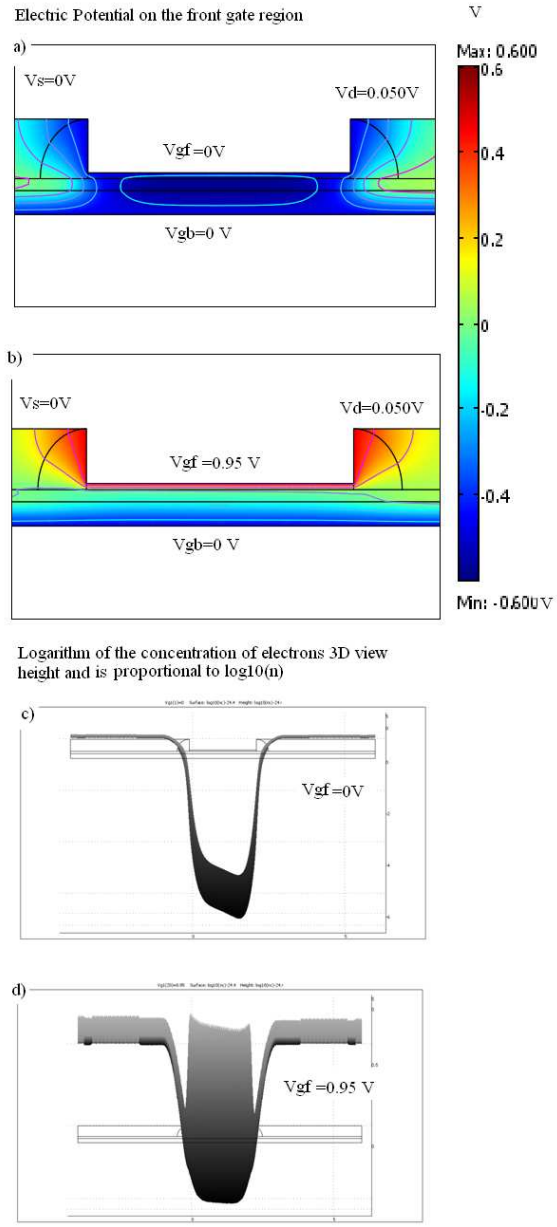

Figure 2: Potential on the front gate region of the device for two different $\mathbf{V_{GF}}$. We set the reference point at $\mathbf{V_s = 0}$. a) $\mathbf{V_{GF} = 0V}$ b)$\mathbf{V_{GF} = 0.95V}$. Figures c) and d) are the logarithm of the concentration of electrons for the gate voltages of a) and b). Notice that when $\mathbf{V_{GF} = 0V}$ the concentration of electrons is several orders of magnitude less than when $\mathbf{V_{GF} = 0.95V}$. c) and d) illustrate how a channel is formed.

The concentration of electrons and holes is not constant since there is a recombination rate, which is given by Shokcley-Read-Hall coefficient R_{SRH}.

$$-\nabla J_p = qR_{SRH} \tag{4}$$

$$-\nabla J_n = -qR_{SRH} \tag{5}$$

$$R_{SRH} = \frac{\sigma_n \sigma_p v_{th} N_t \left(pn - n_i^2\right)}{\sigma_n \left(n + n_i\right) + \sigma_p \left(p + n_i\right)} \tag{6}$$

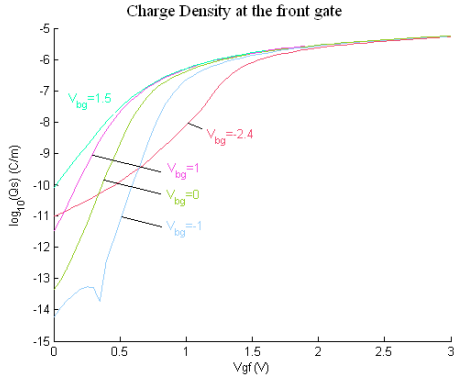

Figure 3: Charge Carrier density at the gate.The charge changes several orders of magnitude due to changes in the $\mathbf{V_{FG}}$. The charge is also infuenced by $\mathbf{V_{BG}}$

The geometry used is described in Figure 1. The concentrations on the substrate is $N_a = 5 \times 10^{17} cm^{-3}$ and the concentration on the gate and the source is $N_d = 1 \times 10^{19} cm^{-3}$. The front oxide thickness is 5nm, the silicon channel thick- ness is 10nm, the back oxide thickness is 20nm. The gate length is 200nm. The actual potential takes into account the electronic affinities of the polysilicon of the gate and the silicon of the bulk, so the potential is not necessarily equal to the gate voltages at the gates. Given the concentrations and the dimensions used, the transistor is Fully Depleted for all the voltages used. This condition is important since the two gates do not interact if the transistor is not fully depleted. For the depletion and the weak inversion regimes, the depletion layer has a width described by equation 7.

$$W_D = -\frac{\epsilon_s}{C_i} + \sqrt{\frac{\epsilon_s^2}{C_i^2} + \frac{2\epsilon_s \left(Vg - \phi_{ms}\right)}{qN_A}} \qquad (7)$$

Using this equation and the data from the model, we obtain that the transistor is fully depleted from $V_{GF} = -0.42V$. For all positive voltages, the silicon region on the transistor does not have holes.

Results

The model provides the potential profile in all the device as can be seen in Figure 2. We can also see that the concentration of electrons increases drastically at the gate when a voltage in the front gate $V_{GF} > V_{th}$ is applied. We are interested on the charge at the gate, since conduction will only happen if an inversion layer is present. We define the charge of the carriers at the gate in Equation 8. We will integrate over the silicon oxide interface boundary, from the drain to the source.

$$Q_s \equiv \int_{gate} q\left(p - n - N_a\right) ds \qquad (8)$$

where s is the arc length. We integrate at the interface of the oxide using various V_{GB} and we obtain Figure 3. It shows how charge accumulates at the gate and at V_{th}, charge goes up drastically forming a channel.

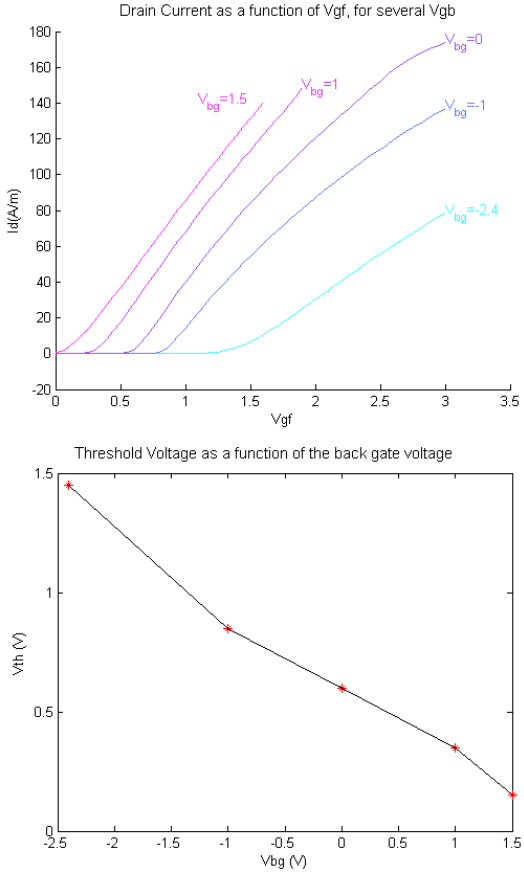

Figure 4: Drain Current as a function of $\mathbf{V_{FG}}$. Notice that the voltage at which the device is turned on can be controlled by $\mathbf{V_{BG}}$. b)Threshold Voltage as a function of the back gate voltage. Note the linear relationship.

The drain current is calculated as $I_d = \int_{drain} \left(J_n + J_p\right) ds$. The behavior of the current in a SOI-MOSFET is similar to a regular MOSFET but it has a shift on the voltage axis. As can be seen in the Figure 4, the device turns on at different V_{th}, depending on the V_{GB} applied. We extracted the Threshold Voltage using the Extrapolation in the linear region method [7] for each of the curves presented on Figure 4 to find the dependence of V_{th} on V_{GB}. As can be seen, the relationship is linear. This dependence has been reported experimentally by [2] and theoretically by [3]. Another parameter that we can use to validate the model is the transconductance. We find it using equation 9.

$$g_m = \frac{dI_d}{dV_{GF}} \qquad (9)$$

The transconductance measures then the rate of change of the current with respect to the gate voltage. A model for the transconductance has been developed by [8] for regular MOSFETs. The curves obtained in the present work are similar when the channel is not fully depleted, however we can see that the transconductance depends on the back gate voltage when depletion is complete. Figure 5 b sugests that the transconductance peak can be maximized changing V_{BG}.

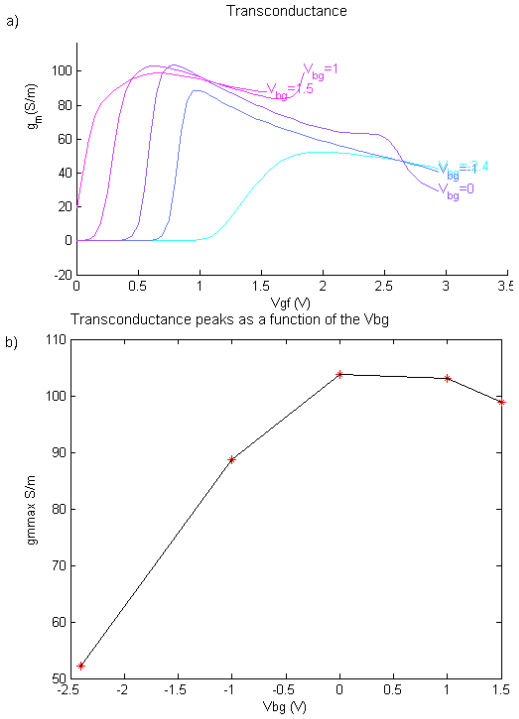

Figure 5: Transconductance of the device. Notice how the peak varies in Figure a) and that is summarized in Figure b)

Conclusions

We have presented a model that simulates an UT-FD-SOI-MOSFET using COMSOL Multiphysics. The model simulates the Electrostatic potential and the drift and diffusion currents on the device using Poisson equation and Drift and Diffusion equations for the charge carriers. We extracted the Threshold Voltage dependence on the back gate voltage and it agrees with experimental results. We have also presented the dependence of the transconductance on the back gate voltage and the basic form agrees with experimental results from a larger SOI-MOSFET. The variation of the transconductance due to the back gate voltage is shown and agrees with the results already reported in literature [9] for larger devices, however that study does not extend to ultra thin transistors. The found relationship between the back gate voltage and the transconductance suggest a dependence of g_m of V_{GB} and that g_m can be maximized using the V_{GB}. The results we have obtained validate the model for the conditions that we have considered.

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