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# TCAD Simulation for ultrathin body and buried oxide fully depleted silicon-on-insulator MOSFET: a comparison between COMSOL and Sentaurus

# Simulación TCAD para un MOSFET de silicio en aislante, ultra fino con óxido enterrado y completamente agotado: una comparación entre COMSOL y Sentaurus

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**Abstract**

In the present work, we develop a model for simulating an ultrathin body (10nm) and buried oxide (20nm) fully-depleted silicon-on-insulator MOSFET with $SiO_2$ gate oxide (5nm) by using TCAD-*Sentaurus* software. We performed DC-simulations for studying the behavior of the threshold voltage and the transconductance. Furthermore, AC-simulations were performed for studying the inversion capacitance and the inversion charge. We compare our results with similar simulations carried out in a previous work in which *COMSOL-Multiphysics* software was used. We have obtained similar results in both works. However, *Sentaurus* features more interesting details like introducing a more realistic picture of the physical mechanisms of such complex devices.

**Keywords.** SOI-MOSFET, TCAD-simulation, Sentaurus, Poisson's equation, drift-diffusion equations.

**Resumen**

En el presente trabajo, se desarrolla un modelo para simular un dispositivo MOSFET de silicio en aislante, ultra delgados con oxido enterrado (20m) y agotados completamente con $SiO_2$ (5nm) como compuerta. El software que se usa es TCAD-*Sentaurus*. Se desarrollaron simulaciones DC para estudiar el comportamiento del voltaje de encendido y la transconductancia. Además, se desarrollaron simulaciones AC para estudiar la capacitancia y carga de inversión. Los resultados fueron comparados con un trabajo previo en el que se usó como simulador al programa *COMSOL-Multiphysics*. Los resultados obtenidos son muy similares entre ambos trabajos. Sin embargo, *Sentaurus* ofrece características más interesantes como introducir modelos más reales para los mecanismos físicos de dispositivos complejos.

**Palabras Clave.** SOI-MOSFET, simulación TCAD, Sentaurus, ecuación de Poisson, ecuaciones de difusión y deriva.

## Introduction

Complementary metal-oxide-semiconductor (CMOS) technology is the base of actual electronics. The scaling of the metal-oxide-semiconductor field effect transistor (MOSFET) has allowed great advances in the semiconductor industry related to the increase of the transistor density and the development of high performance systems that consumes less power [1–6]. However, short channel effects (SCE) related to transistor scaling have detrimental effects on the overall performance. The most serious effects are the variation of the threshold voltage ($V_{th}$) with the length channel and the drain induced barrier lowering (DIBL) [1–6]. That is the reason why it was developed CMOS with novel architecture such as the Fully Depleted Silicon-on-Insulator (FD-SOI) MOSFET.

Indeed, the presence of SCE on SOI technology are reduced. Further, this technology features interesting advantage such as higher speed, lower power consumption, advanced scalability and less parasitic effects [2–4]. However, such devices are based on coupling effects between the front and back channels. This produces a high degree of complexity for understanding SOI devices. That is the reason why it is necessary to inter-

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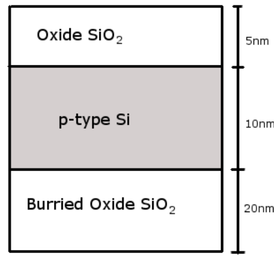


**Figure 1: Transversal structure of the simulated UTFD-SOI-MOSFET device.**

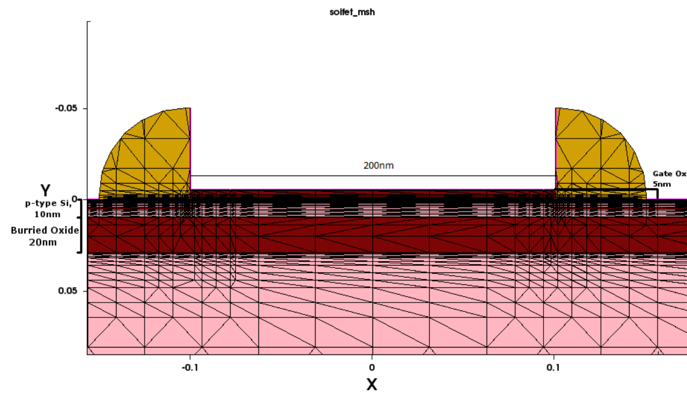


**Figure 2: Gate and channel structure with the mesh.**

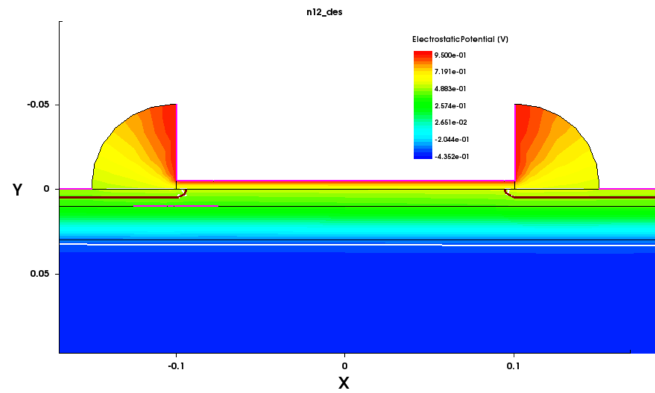


**Figure 3: Electrostatic potential for the configuration: $V_G$=0V and $V_D$=50mV. No channel is formed.**

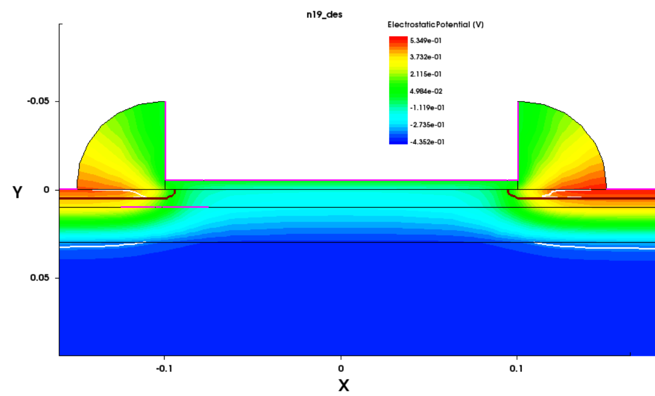


**Figure 4: Electrostatic potential for the configuration: $V_G$=0.95V and $V_D$=50mV. A channel is formed.**

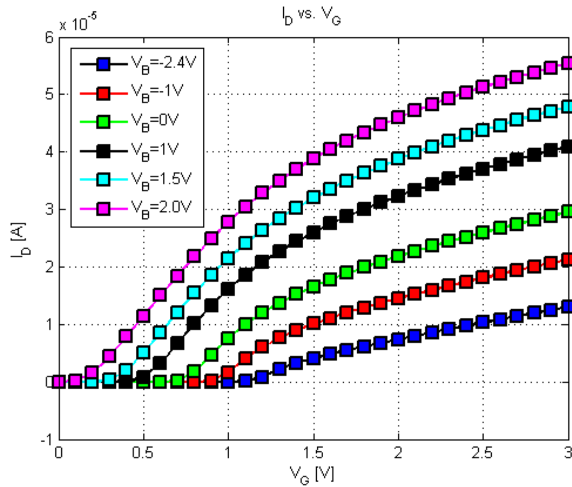


**Figure 5: $I_D$-$V_G$ curves for different VBG voltages.**

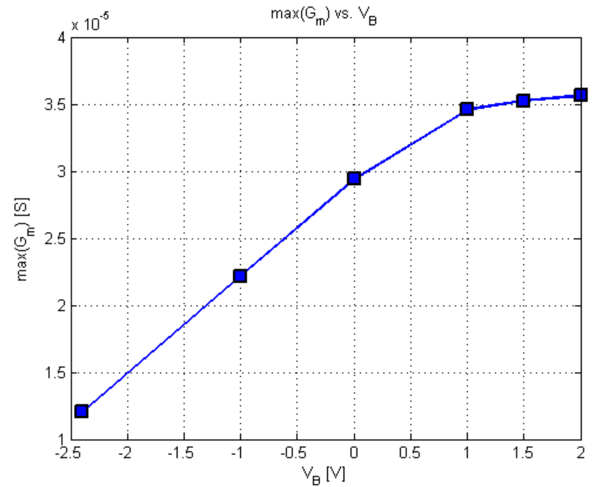


**Figure 8: Peak of $G_m$ vs. $V_{BG}$. The curve seems to stabilize around 2.0V.**

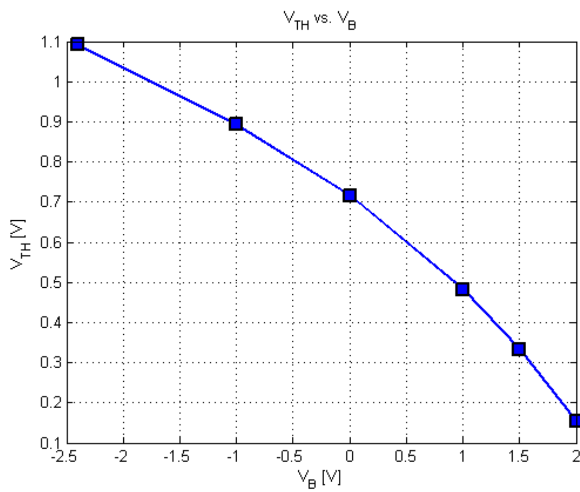


**Figure 6: $V_{th}$ vs. $V_{BG}$. We can see a clear dependency and an inverse correlation.**

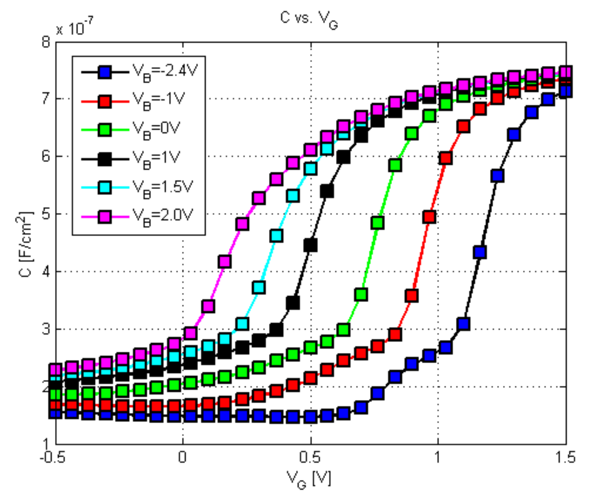


**Figure 9: Inversion capacitance vs. $V_G$ for different $V_{BG}$ voltages.**

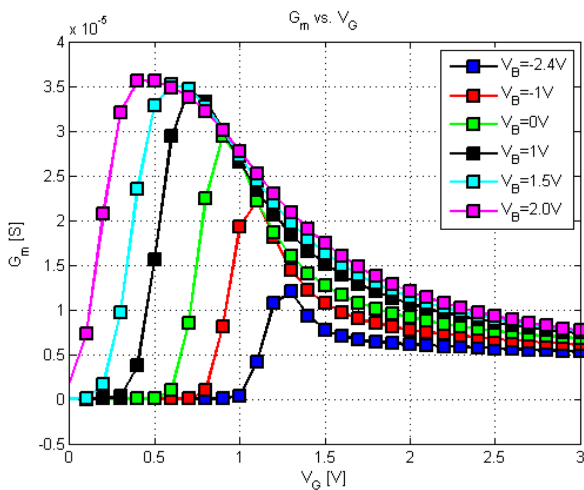


**Figure 7: $G_m$ vs. $V_G$ for different $V_{BG}$ voltages.**

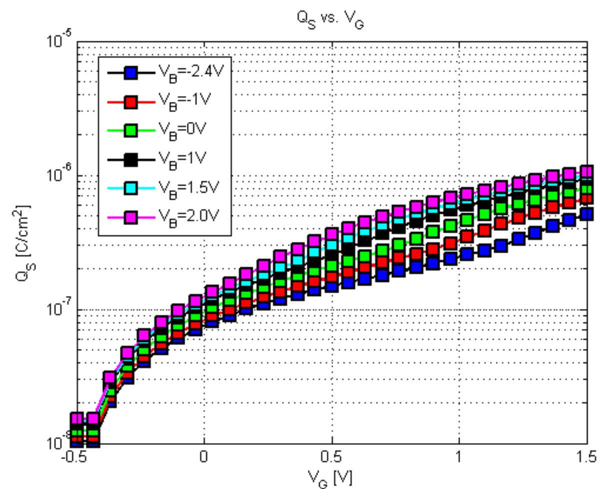


**Figure 10: Surface charge vs. $V_G$ for different $V_{BG}$ voltages.**

pret the experimental data with simulation. The usual software for this kind of work is a TCAD (Technology Computer Aided Design) simulator.

In a previous work, we already made a model of a FD-SOI MOSFET by using *COMSOL-Multiphysics*. In this work, we aim to make a similar model using *Sentaurus* and compare the results in order to show that *Sentaurus* give a more realistic picture of a FD-SOI MOSFET. Therefore, we simulate a FD-SOI MOSFET by using *Sentaurus* with the same structural model developed in [5] and we perform DC and AC studies. Particularly, we analyze the drain current, the transconductance, and the capacitance for different back-gate voltages. As well, we study the electrostatic potential for different gate voltages in order to analyze the channel formation. Finally, we discuss the results with our previous works already presented in [5, 6].

## Methodology

The transversal structure of the studied FD-SOI-MOSFET consists of $SiO_2$ (5nm)/p-type Si (10nm)/$SiO_2$ (20nm) as we can see in Figure 1. A 2D model was developed for the device with an effective channel length of 200nm. The doping concentration of the source and drain regions is $N_D$=1E19 cm$^3$ (phosphor) and the substrate concentration is $N_A$=5E17 cm$^3$ (boron). A Gaussian distribution is used for the transition between the drain (or source) region and the p-type-Si region. *Sentaurus-Structure-Editor* [7] was used for creating the geometry, concentrations and the mesh of the device (Figure 2). The simulations were performed by using *Sentaurus-Device* which solve the Poisson's equation [8]:

$$\nabla\left(\varepsilon\nabla\phi\right) = -e\left(p - n + N_D - N_A\right) \qquad (1)$$

where $\phi$ is the electrostatic potential, $\varepsilon$ is the electrical permittivity, *e* is the elementary electron charge, *p* is the hole density, *n* is the electron density, $N_D$ is the concentration of the ionized donors and $N_A$ is the concentration of the ionized acceptors. Poisson's equation is coupled with the drift-diffusion equations [8]:

$$J_n = \mu_n\left(n\nabla E_C - 1.5nKT\nabla\ln m_n^*\right) + D_n\left(\nabla n - n\nabla\ln\gamma_n\right) \qquad (2)$$

$$J_p = \mu_p\left(p\nabla E_C - 1.5pKT\nabla\ln m_p^*\right) + D_p\left(\nabla p - p\nabla\ln\gamma_p\right) \qquad (3)$$

where $E_C$ and $E_V$ are the conduction and valence bands edges, $\mu_n$ and $\mu_p$ are respectively the electron and hole mobilities, $m_n^*$ and $m_p^*$ are the electron and hole effective masses, $D_n$ and $D_p$ are the electron and hole diffusion coefficients, *p* and *n* are the hole and electron densities, $\gamma_n$ and $\gamma_p$ are coefficients related to the Fermi statistics and *T* is the temperature [8].

Moreover, the Shockley-Read-Hall model is used for electrons and holes recombinations [8]. Since we perform a 2D simulation, an area factor equal to 1$\mu$m was used as transistor width. For mobility models, we have used the Philips unified model [7, 9] together with the Lombardi's model for thin layers [7, 10, 11]. Finally, quantum corrections are taken in to account in these simulations [7].

## Results

The electrostatic potential is showed in Figures 3 and 4 for several gate and drain biases. In Figure 3 ($V_G$=0V and $V_D$=50mV), the channel is not formed while it is in Figure 4 ($V_G$=0.95V and $V_D$=50mV) consistent with the biasing. In Figure 5, we show the DC-analysis ($I_D$-$V_G$ simulations) for different back-gate voltages ($V_{BG}$). The variation of the $I_D$-$V_G$ curves agrees with our previous work presented in [5]. In the same way, the variation of the threshold voltage ($V_{th}$) with respect to $V_{GB}$ (Figure 6) is consistent with works presented in [5, 12, 13]. Note that $V_{th}$ was extracted by using the method of the maximum of the transconductance explained in [14]. In Figure 7, the transconductance, $G_m$, is plotted in function of $V_G$ and in Figure 8 the maximum of $G_m$ is plotted as a function of $V_{BG}$. We can clearly see that $G_m$ depends on $V_{GB}$ which agrees with [5, 6, 15]. Further, in all these simulations, both TCAD softwares: *Sentaurus* and *COMSOL* have very similar results.

However, a great difference between *COMSOL* and *Sentaurus* is the possibility of performing AC-analyses such as C-V simulations, in which a small-signal in a specific (or variable) frequency is connected to one of the transistor's terminals and then, the admittance matrix is measured [8]. Figure 10 shows the capacitance as a function of $V_G$ for different $V_{BG}$ which agree with an experimental previous work presented in [6]. We can also observe that the oxide capacitance ($C_{OX}$) is consistent with the dielectric thickness. Further, the capacitance clearly depends on $V_{BG}$. By using the C-V curves, we can easily obtain the inversion charge, $Q_S$, as we show in Figure 11. Note that in [5], the inversion charge was extracted by using the integration of the local value of the inversion charge in the channel.

## Conclusions

The simulation of a FD-SOI-MOSFET was accomplished successfully by using *Sentaurus*. This model solves the Poisson's equation coupled with the drift-diffusion equations. We have obtained $I_D$-$V_G$ curves for different $V_{GB}$ voltages. From these curves, the values of $V_{th}$ were extracted and its tendency with respect to $V_{BG}$ agrees well with experimental results. The peak of $G_m$ was studied and its behavior with respect to $V_{BG}$ also agrees with experimental results. Although *COMSOL* and *Sentaurus* renders really similar results, *Sentaurus* enables a more precise extraction of the capacitance by

using an AC analysis. The validity of this extraction was confirmed by the behavior of the capacitance in function of $V_G$ for different $V_{BG}$ and the Cox value. Finally, this model produces successful simulations and can be used for future works in complement with experimental studies. Moreover, *Sentaurus* enables to simulate a device from the manufacturing process (*Sentaurus-Process*), a useful tool that will be explored in future works.

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