

Thermal-Electrical finite element analysis of nanometric copper vias under high fluence stress

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Abstract

This paper presents the development of a thermal-electrical finite element (FE) model with the objective to analyze failure mechanisms responsible of physical degradation (void, copper silicate formation, etc.) caused by high fluence stress of 90nm copper vias for FinFET devices. Indeed in [1], this physical degradation was interpreted as a main consequence of Joule effect, however their employed model reached too low temperatures to explain the observed physical degradation. In order to confirm this, the steady-state FE model developed in this work computes the temperature increase and distribution caused by high electrical current density flowing through a copper contact, considering non-ideal thermal and electrical interfaces. In addition, a sensitivity analysis is performed as a way to identify critical failure parameters. The temperature response of the model to independent variation of electrical resistivity of studied materials, and interfacial electrical and thermal conductance between the copper contact and its diffusion barrier were obtained. The decrease of interfacial electrical conductance triggers steady-state temperatures over copper and silicate melting points and, in consequence leads to temperature high enough to explain the physical degradation.

Keywords. copper nano vias, Joule heating, finite element analysis, interface electric conductivity, sensitivity analysis.

Resumen

Este trabajo presenta el desarrollo de un modelo termo-eléctrico de elementos finitos (EF) con el fin de analizar los mecanismos de falla responsables de la degradación física causada por alta densidad de corriente en contactos de cobre de 90 nm empleados en dispositivos FinFET. De hecho en [1], esta degradación física fue interpretada como consecuencia principal del efecto Joule, sin embargo el modelo empleado alcanzó temperaturas demasiado bajas comparadas con el daño observado. Con el propósito de confirmar esta hipótesis, el modelo de EF de estado estable desarrollado en este trabajo calcula el incremento y la distribución de temperatura causada por alta densidad de corriente eléctrica fluyendo a través de un contacto de cobre, tomando en cuenta interfaces eléctricas y térmicas no idealizadas. Además, un análisis de sensibilidad fue realizado como un medio para identificar parámetros críticos de falla. La respuesta del modelo ante la variación independiente de la resistividad eléctrica de los materiales estudiados, y las conductancias eléctricas y térmicas entre el contacto de cobre y su barrera de difusión fue obtenida. La disminución de la conductancia eléctrica de dicha interfaz desencadenó temperaturas de estado estable superiores a los puntos de fusión del cobre y los silicatos del contacto y, en consecuencia, permite explicar la degradación física observada.

Palabras Clave. nano contactos de cobre, calentamiento Joule, análisis de elementos finitos, conductividad eléctrica de interfaz, análisis de sensibilidad.

Introduction

Ongoing MOSFET scaling has led to consider new architecture like FinFET (FF), three dimensional devices with new dielectric materials such as high dielectric constant (high-k) materials [2, 3]. This has implied further

reduction of contact dimensions, which now reaches diameters of less than 50 nm [4, 5]. These "nano vias" are of the utmost importance to get the best performance of the FF, mainly because of series resistance and parasitic capacitance considerations.

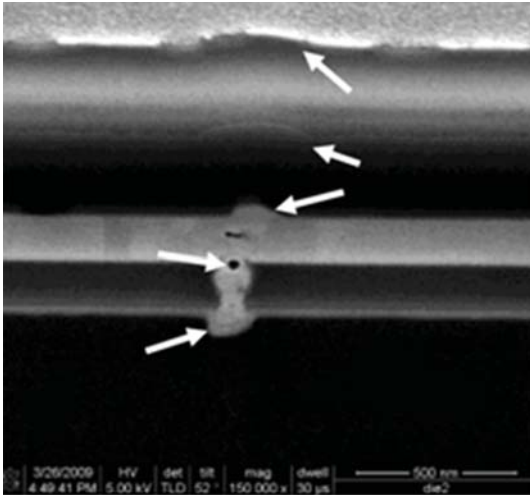


Figure 1: Severe damage in stressed Cu via. Voiding, copper silicide formation and considerable distortion is observed. (Figure included in [1]).

Recently, during several failure tests, it has been observed that copper nano vias are literally destroyed (Figure 1) under high fluence stress [1–6]. This may find an explanation by localized heating due to Joule effect, but first order calculations based on simplified thermal considerations show rather low temperature in order to explain void presence in the nano vias, which such be over, at least, copper silicate formation temperature (823 K) [1–7]. In order to assure reliability and improvement on nano scales, it is necessary to understand the degradation process of these devices. The aim of this work is to identify failure mechanisms of copper nano vias through a thermal-electrical finite element (FE) model based on experimental data obtained in [1]. First we will develop a FE model considering exact contact geometry and non-ideal thermal and electrical interfaces, and then the temperature increase caused by an applied electrical current load of 157 MA/cm² will be computed and related to observed damage. Finally, as a way to identify failure mechanisms, a sensitivity analysis will be performed varying electrical resistivity and interfacial properties of the contact.

Methodology

Thanks to its capability to handle non-trivial geometries, loads and interactions, FE analysis is a commonly used approach to solve thermal-electrical problems. In this specific case, Joule heating in the vias was modeled employing the commercial FE software package Abaqus/Standard [8]. Temperature failure was simulated and compared to experimental observations.

During Joule heating, electrical conductivity is usually a function of temperature, and internal heat generation is a function of electrical current density. This close coupling between the electrical potential and the temperature fields demands the solution of both of them simultaneously. In this context, Abaqus/Standard allows to analyze the phenomenon through a fully coupled thermal-

electrical procedure [8]. This procedure combines both transient and steady-state heat transfer processes (such as convection, gap conductance and contact resistance) with steady-state electrical processes (such as current flow and surface resistance).

In general, both fields of this problem are coupled considering local Joule Law, that defines the rate of electrical energy P_{ec} dissipated as thermal energy as:

$$P_{ec} = J \cdot E \quad (1)$$

, where J is the electrical current density and E the electric field amplitude. Relating these terms to the electric potential field, P_{ec} could be expressed as:

$$P_{ec} = J \cdot E = \frac{\partial \varphi}{\partial x} \cdot \sigma^E \cdot \frac{\partial \varphi}{\partial x} \quad (2)$$

, where $\sigma^E(\theta, f^\alpha)$ is the electrical conductivity matrix, σ is the temperature and $f^\alpha, \alpha = 1, 2 \dots$ are predefined field variables [8]. Thus, the heat generated is a function of the electric potential field and both problems are coupled. It should be noted that the amount of this energy released as internal heat is $r = n_v P_{ec}$ where n_v is the energy conversion factor, also known as the Joule heating factor. In this case, the Joule heating factor is considered to be 0.9, a conservative approximation [8].

Model inputs

During experiments described in [1], copper Kelvin structures of 90 nanometers with a 10 nanometer diffusion barrier of tantalum nitride TaN were tested. The resistance of a single via was measured to be about 22 ohms. A constant current of 10 mA, corresponding to a current density of 157 MA/cm², was forced through the Cu vias. Based on these conditions, an axis-symmetrical model of the vias was developed. The geometry consisted in a distribution of layers composed of several materials. Each layer was defined as an independent component, and thermal and mechanical interactions between each of them were adequately specified (Figure 2a). The vertical axis of the vias was defined as a symmetry line for the axis-symmetrical mesh (Figure 2b).

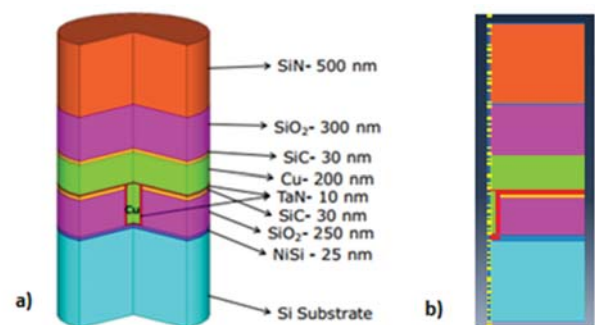


Figure 2: a) Layer distribution and vias projected geometry [1] b) Simplified axis-symmetrical geometry.

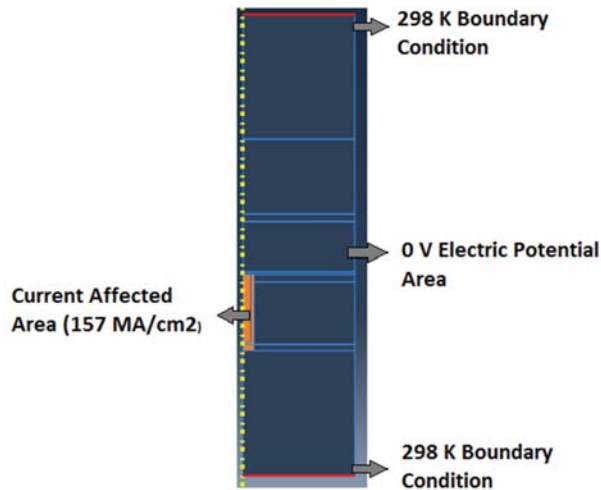


Figure 3: Boundary conditions and loads for FE model.

Two analogous contacts of 80 nm and 90 nm diameter were modeled under these conditions. In the first case the system's mesh was composed of 8,806 coupled heat transfer and electrical quadratic elements and 27,197 nodes. In the case of the 90 nm vias, the mesh was composed of 8,807 elements and 27,198 nodes.

Both electrical and thermal material properties are based on real measurements performed before the actual experimental process. It was difficult to obtain adequate temperature-dependent nano-scale properties during the realization of the tests. In consequence, the bulk material properties employed for this work are taken from [1], these parameters were measured on a macroscopic scale independently of temperature. These values are summarized in Table 1.

For realistic modeling, only the vias core was subjected to a 10mA electrical current flowing from the Cu and TaN region to NiSi region. This value was applied as an equivalent current density load on the top of the Cu layer on both simulated contacts. Boundary conditions of null electric potential were applied to the rest of the contact in order to confine current flow and heat generation to this desired region (Figure 4). Regarding heat transfer conditions, a prescribed temperature of 298 K was applied to both contact ends. Also an initial temperature of 298 K was applied through the whole region. Due to the reduced scale of the contact, the effect of convection and radiation processes are negligible (Figure 3). Similar models developed in previous research showed good fit between experimental and simulation results for less extreme current densities [9, 10].

Since the vias core is subjected to a potential gradient on both extrema, an equivalent electrical circuit with several resistive elements describes it. Cu and TaN layers could be considered as two resistive elements arranged in parallel between each other, and NiSi layer as an element arranged in series with both of them (Figure 4). The total electrical resistance value of this circuit is expected to be consistent with the overall electrical

resistance measured during the experimental tests (22 Ω). Based on the geometric characteristics and resistance of individual materials, it was noted that a contact resistance in the TaN/NiSi interface (17.3 Ω for 80 nm contact and 18.4 Ω for 90 nm contact) must be included to achieve the overall measured value. This value is consistent with evidence that indicates strong dependency between interface resistance and cleaning process [11, 12]. Besides this condition, every other interface was supposed to have an ideal behavior.

Model outputs and sensitivity analysis

Steady-state temperature and current density distributions inside the contact were computed as the main model outputs. The resulting temperature profile was expected to be consistent with the melting failure mode observed during testing.

Since macroscopic material properties were used, it is necessary to understand the effect caused by variation of some key parameters over the system. For this goal, a parametric study of the following characteristics was performed:

- Cu Electrical Conductivity.
- TaN Electrical Conductivity
- NiSi Electrical Conductivity.
- NiSi/TaN interface Electrical Conductance.
- NiSi/TaN interface Thermal Conductance.

Each material property value was reduced independently and system temperature response was calculated. The theoretical values provided included in Table 1 were used as base parameters.

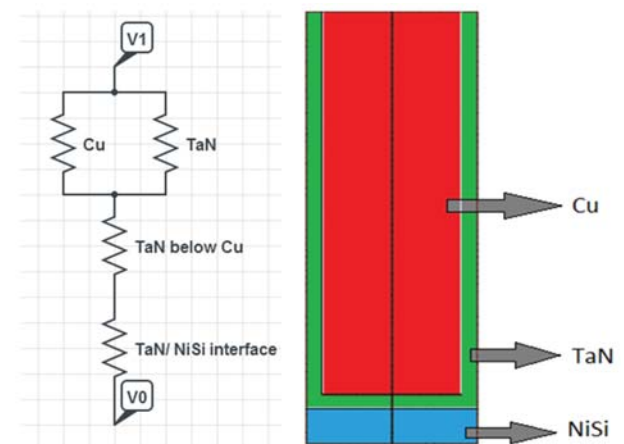


Figure 4: Equivalent circuit of contact core.

Material	Cu	Si	SiO ₂	SiC	SiN	NiSi	TiN	TaN
Thermal Conductivity [W/m · K]	401	120	1.4	1.4	28	135	28.84	135
Electrical Resistivity [Ω · m]	3e-8	2e14	1e+14	1e14	1e14	6e-8	3.5e-6	1.0e-6

Table 1: Thermal conductivity and electrical resistivity of materials considered in the model.

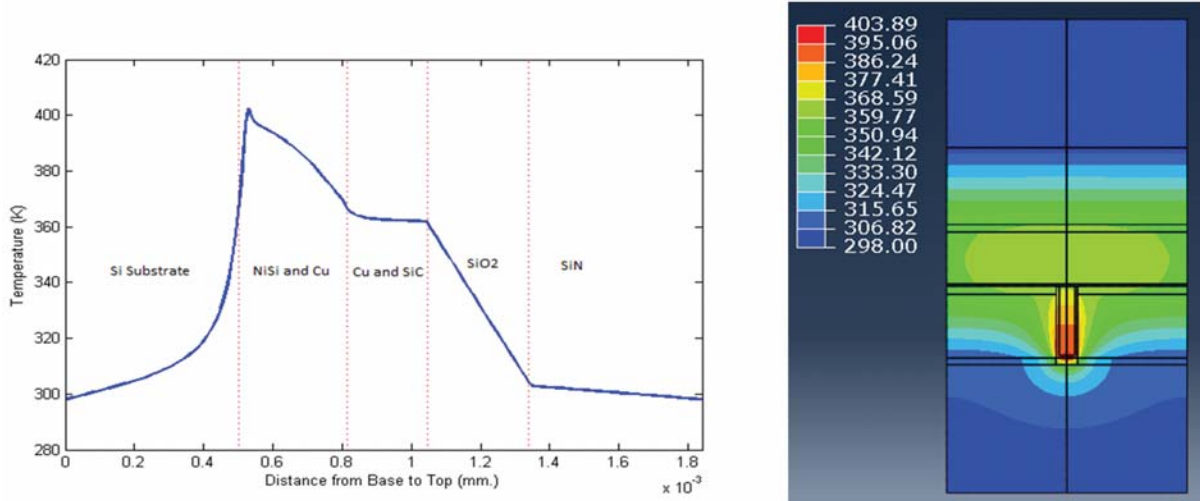


Figure 5: Temperature (K) profile and distribution for 80 nanometer contact.

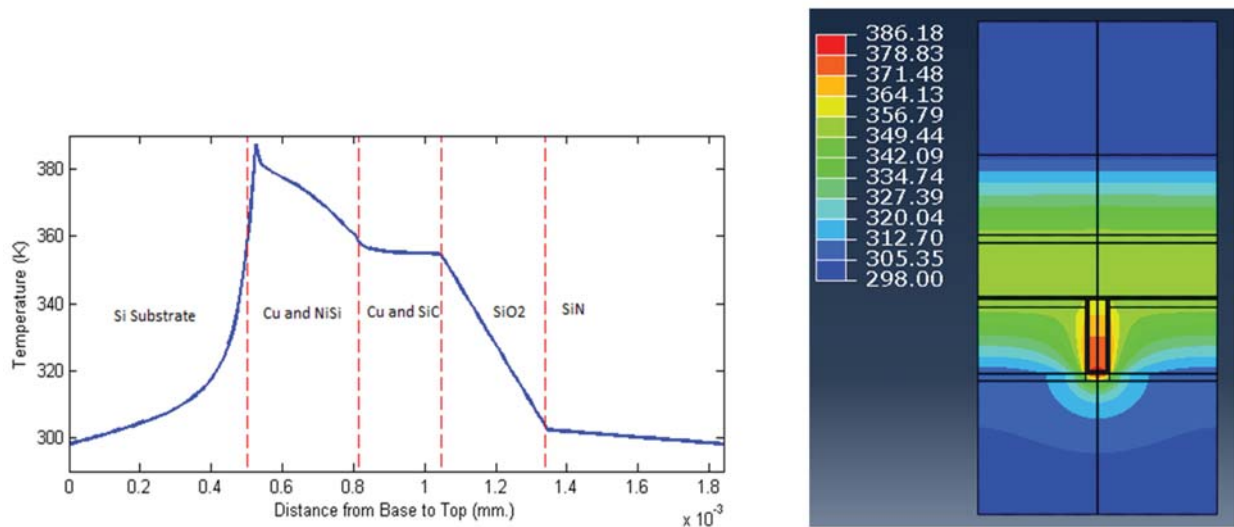


Figure 6: Temperature (K) profile and distribution for 90 nanometer contact.

Results and Discussion

Steady-state temperature profiles were computed for both 80 nm and 90 nm contacts (Figure 5, Figure 6). The temperature increment is not enough to reach melting temperatures as observed during the experimental procedure, neither in the copper region nor in the silicate region as also in [1].

A possible explanation for this behavior relies on uncertainty of material parameters and justifies the sensitivity analysis. Previous analysis have shown a similar tem-

perature increase when temperature dependency of material properties on nanometric scale is not considered [9, 10]. Besides this temperature underestimation, the overall temperature profile and the location of the highest temperature value are consistent with experimental conditions. The effect of different thermal conductivities and non uniform current density distributions in the system is clearly noted.

Regarding the sensitivity analysis, the maximum steady-state temperature was computed as a fraction of the orig-

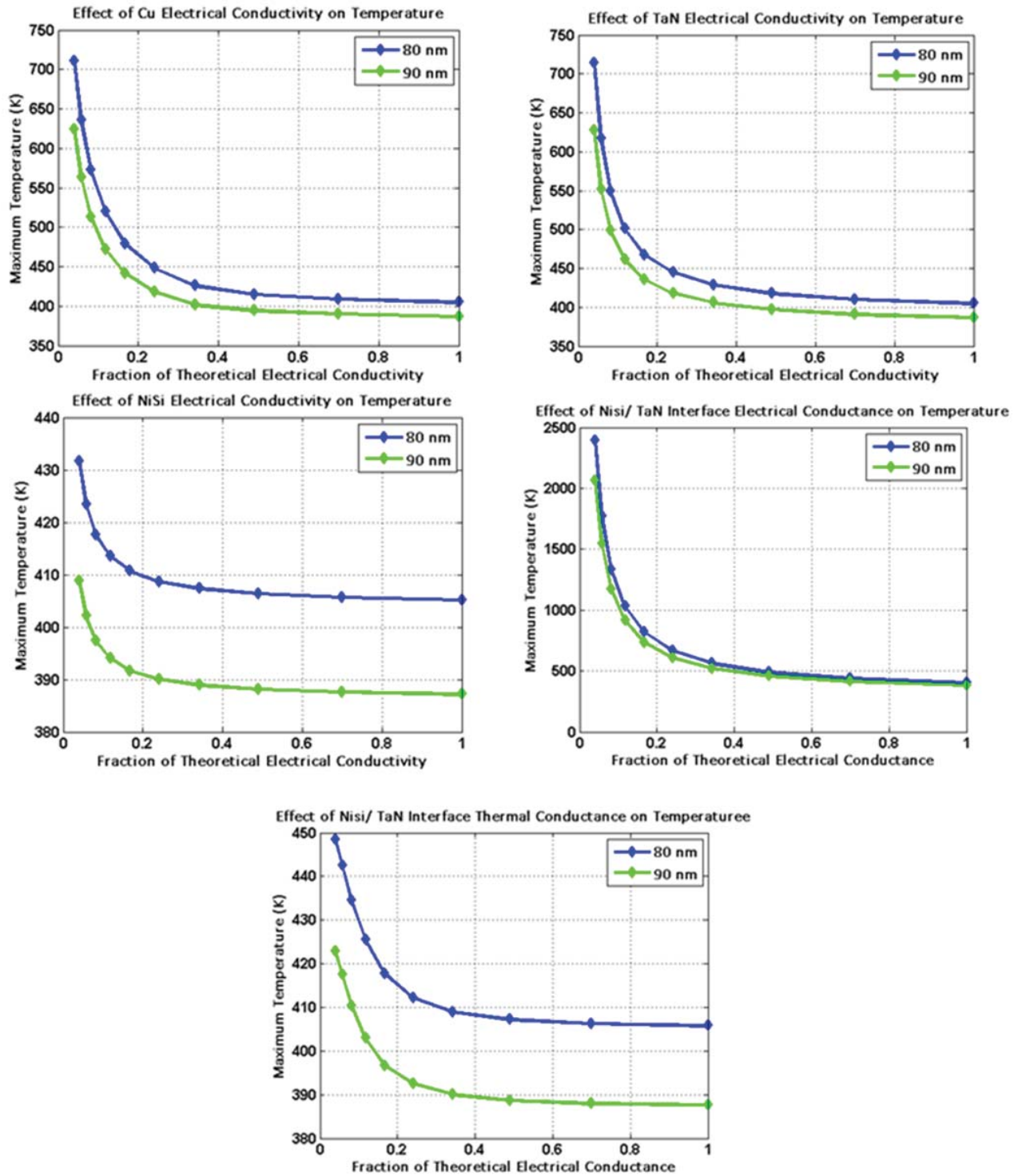


Figure 7: Maximum temperature (K) for varying model parameters.

inal parameter value for both contact diameters (Figure 7).

NiSi/TaN interface electrical conductance was identified as a main heat source. Melting temperatures could be reached with reduction in its value: below 10% of theoretical magnitude. The change in other model parameters such as electrical conductivity and thermal conductance does not affect the final temperature in the

vias in a significant way. In consequence, the sustained growth of electrical resistance in the interface between NiSi/TaN shall be considered as one of the main failure mechanisms in this case. A similar surface effect has been noted during simulation of Cu nanowires in [13]. However, a physical explanation for change of this parameter is missing. An appropriate interface simulation and more accurate material properties measure-

ments would be useful to clarify it [10, 13]. A relation between NiSi/TaN electrical conductance and NiSi/TaN thermal conductance should also be expected.

In addition, a very restrictive factor for the final steady-state temperature obtained is related to the constant temperature boundary conditions applied on both contact extremes. These fixed temperatures do not account for physical behavior and could act as heat sinks [14]. Future work should include more realistic boundary conditions.

In addition, is evident that the difference between the 80 and 90 nm diameter contacts is mainly a geometrical effect. Since the 80 nm contact has higher resistance than its 90 nm counterpart (*due to a lower diameter*), the temperature increase is larger.

Conclusions

A thermal-electrical FE model of Joule heating in nanometric copper vias was developed. Geometrical, physical and interface characteristics were implemented on detail in an attempt to emulate the physical behavior under high fluence stress. In addition, two different vias diameters were considered.

The final temperature increase due to Joule heating in both cases wasn't enough to account for the melting failure observed during testing. However, a sensitivity analysis allowed recognizing NiSi/TaN interface electrical conductance as key parameter to trigger high temperatures over copper and silicides melting points. In quantitative terms, it was observed that the magnitude of electrical conductance should decrease to approximately a 10% of its theoretical value in order to achieve such temperatures. This process of electrical conductance decrease is not fully understood through FE modeling and an interface theory should be applied in future work in order to clarify it. In addition, more physically meaningful boundary conditions should be implemented in the model. Finally the scaling led to reduce the diameter of the nano vias, turning heat generation and operative current conditions of FinFET into real technical challenges.

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