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EN CIENCIAS E INGENIERÍAS
ARTÍCULO/ARTICLE SECCIÓN/SECTION C

Mobility extraction in ultra thin, body buried oxide and fully depleted silicon-on-insulator MOSFET

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Editado por/Edited by: Cesar Zambrano, Ph.D.
Recibido/Received: 06/05/2013. Aceptado/Accepted: 01/06/2013.
Publicado en línea/Published on Web: 28/06/2013. Impreso/Printed: 06/06/2013.

Abstract

In this paper, we extract the mobility of ultra-thin, body buried oxide and fully depleted silicon-on-insulator MOSFET, for different front and back-gate configurations. The mobility values are found by using the Capacitance - Gate Voltage and Current - Gate Voltage characteristics. In addition, the maximum electron mobility is calculated for both configurations: SiON/Si (front-gate) and SiO_2/Si (back-gate). Based on the mobility peak, it is determined that the electron transport can be improved by a factor of 1.6 for the front gate configuration. This improvement is explained by the back-channel activation. On the other hand, for the back-gate configuration the electron mobility is improved by a factor of 2.5. A second peak is observed in the electron mobility but cannot be appreciated, mainly because of the influence of an additional capacitance.

Keywords. UTBB-FD-MOSFET, silicon-on-insulator, mobility, front-gate configuration, back-gate configuration

Resumen

En el presente trabajo, se extrae la movilidad de dispositivos MOSFET de silicio en aislante, ultra delgados y agotados completamente, para las configuraciones de compuerta frontal y trasera. Los valores de movilidad fueron encontrados usando las características Capacitancia - Voltaje de Compuerta y Corriente de Drenaje - Voltaje de Compuerta. Adicionalmente, se calcula el máximo de movilidad de electrones para ambas configuraciones: SiON/Si (compuerta frontal) y SiO_2/Si (compuerta trasera). En base al pico de movilidad encontrado, se determina que el transporte de electrones puede ser mejorado por un factor 1.6 para la compuerta frontal. Esta mejora se explica por la activación de la compuerta trasera. Por otro lado, en la configuración de compuerta trasera la movilidad de electrones se mejora en un factor 2.5. Un segundo pico puede ser observado en la movilidad de electrones, sin poder ser apreciado con claridad y siendo originado por la presencia de una capacitancia adicional.

Palabras Clave. UTBB-FD-MOSFET, silicio en aislante, movilidad, configuración de compuerta frontal, configuración de compuerta trasera

Introduction

The silicon-on-insulator (SOI) technology presents interesting advantages with respect to the bulk silicon in terms of higher speed, lower power consumption, less parasitic effects and advanced scalability [1–4]. This technology has been explored for around 30 years and in the last 10 years, it has been implemented in commercial computer processors [5]. The SOI technology introduces some parameters that can be used for optimization of performance and scaling like the back-gate voltage (V_{G2}) and substrate doping [2–4]. As well, it has been shown that the short channel effects are reduced in ultra-thin SOI MOSFETs [2–4].

In fully depleted (FD) SOI MOSFETs, the back-gate voltage plays an important role in the control of the threshold voltage (V_{TH}) and in the behavior of the drain current (I_D). The strong interface coupling enables to enhance the drain current. The electron mobility is also

ISSN 1390-5384

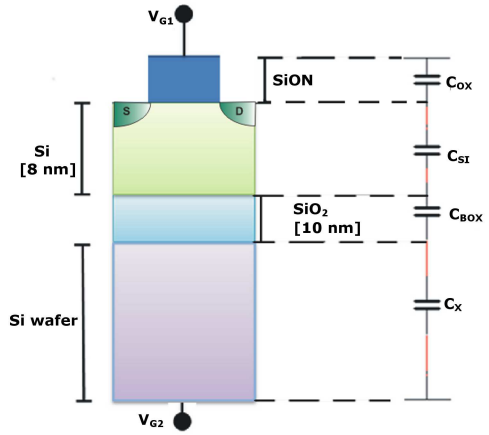

Figure 1: Transversal structure of the used UTFD-SOI-MOSFETs devices (right) and capacitance model (left). In this model, the parasitic capacitance, C_X, is originated by applying a voltage on the back-surface of the wafer.

affected by the back-gate voltage [1–4]. In the present work, we extract the mobility of ultra-thin, body buried oxide and fully depleted SOI MOSFETs (UTBB-FD-SOI-MOSFET) and we study the effects of the back-gate voltage in the electron transport. We also study the electron transport for two configurations: front-gate (or SiON/Si interface) and back-gate (SiO_2/Si interface).

Experimental Description

The UTBB-FD-SOI-MOSFETs devices used during this work have a 10x10 μm area. The front gate dielectric consists of 2.5nm SiON thickness, the body of 8nm of Si with doping of about 10^{15} cm^{-3}and the buried oxide consist of 10 nm of SiO_2 (Figure 1). The Front gate electrode is made of 5nm of TiN with poly-Si cap. The mobility extraction is carried out using the I-V and C-V characteristic method. For the C-V characteristic the Split C-V method was applied [6, 7]. First of all, the mobility of the front gate was extracted for different back-gate biases (V_{G2}), in a range between 0V-5V (step of 0.5V). Then, the back-gate mobility was extracted for various front gate biases (V_{G1}) in a range of 0V-1V (step of 0.1V). Once the source-to-drain current (I_{DS}) and the inversion capacitance C_{inv} were extracted, we assess the mobility by mean of the next expression [8]:

$$\mu_{eff} = \frac{L}{V_{DS} \cdot Q_{inv} \cdot W} I_D \qquad (1)$$

Where L[μm] is the length and W[μm] is the width of the device, V_{DS}[V] is the drain to source voltage, Q_{inv} [C/cm^2] is the inversion charge and I_D [A] is the drain current.

The effective electric field (E_{eff}) in SOI devices can be found using the next expression for the front-gate.

$$E_{eff}^{FG} = \frac{1}{2} Q_{inv}^{FG} \left(1 + \frac{C_P}{C_{FG}} Q_{inv}^{BG}\right) \qquad (2)$$

Where E_{eff}^{FG} is the effective electric field for the front-gate, Q_{inv}^{FG} is the inversion charge in the front-gate, Q_{inv}^{BG} is the inversion charge in the back-gate, C_{FG} [F/cm^2] is the front-gate capacitance and C_P is $C_{FG}//C_{BG}$ (back-gate capacitance). Equation (2) is also used for computing the effective field in the back-gate, just changing the corresponding front-gate parameters and the back-gate parameters.

It is important to mention that the back-gate contact does not use a metallic electrode as the front gate but the p-type well of the Si substrate (below the burrier oxide, Figure 1). This produces extra gate capacitance capacitances that must be considered in the expressions as it will be discussed in great detail in the next section.

Experimental Results

Front-Gate Configuration (SiON/Si interface)

For all measurements done in this configuration, the voltage V_{G2} was varied in a range of 0-5V with 0.5V in every step. Figure 2 shows the C-V characteristic for the SiON/Si interface for different V_{G2}. We can see that there are two rising regions in the curve: the first one is due to the effect of C_{Si} and C_{OX} (Figure 1) and the second one is the value of C_{OX} alone. We have found that C_{OX} = 1.6x10^{-7} F/cm^2. Figure 3 shows the Q_{inv} vs. V_{G1} that is the integral of the C-V characteristic. The $I_D - V_{G1}$ characteristic is shown in Figure 4. Figures 5 and 6 show the μ_{eff} vs. Q_{inv} and μ_{eff} vs. E_{eff}, respectively.

The mobility peak is extracted and plotted in function of V_{G2} in Figure 7. We can see that the maximum peak of mobility occurs at V_{G2}=3V with μ_{eff}=480 cm^2/V.s. This means that the back-gate contribution is able to increase the electron mobility in around 60%. The increase of the mobility peak can be explained by the activation of the back-channel which is consistent with [9]. Apparently, the back-channel is the only one activated, which will be confirmed in next configuration.

Back Gate-Configuration (SiO_2/Si interface)

Figure 8 shows the C-V characteristic for the back-gate configuration. Similarly, the first rising is due to the effect of C_{Si} and C_{BOX} (model in Figure 1). According to the device dimensions and the second rising of the C-V curve in Figure 8, we have: C_{Si}=1.3x10^{-6} F/cm^2 and C_{BOX}=3.3x10^{-7} F/cm^2. The value of the first rising is around C'=1.3x10^{-7} F/cm^2, which cannot be explained by considering only C_{Si} and C_{BOX}. At this point, we have the presence of an additional capacitance: C_X (Figure 1). By using the model presented in Figure 1, we obtain that C_X=2.6x10^{-7} F/cm^2 and that the silicon substrate located below the SiO_2 dielectric (of about 10nm) has a thickness of 40 nm. Figures 9 and 10 show the curves: Q_{inv} vs. V_{G2} and I_D vs. V_{G2}, which are used for the mobility extraction. The transconductance parameter (G_M) is plotted in Figure

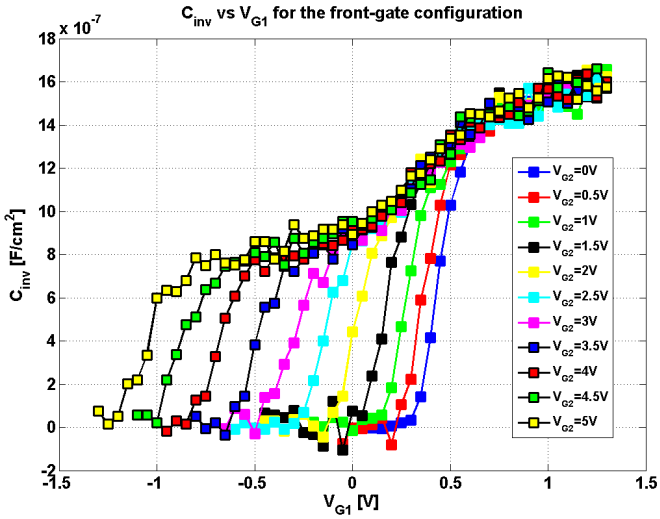

Figure 2: Inversion capacitance (C_{inv}) vs. Front gate voltage (V_{G1}) for the front gate configuration. These parameters are directly extracted from the devices.

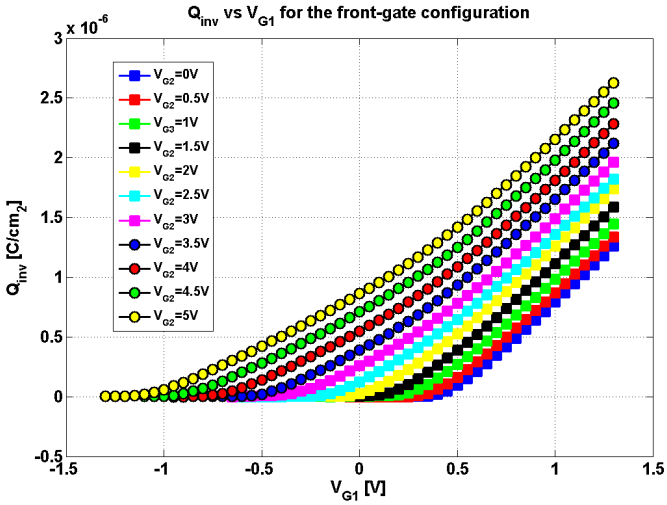

Figure 3: Inversion charge (Q_{inv}) vs. Front gate voltage (V_{G1}) for the front gate configuration. These curves are the result of the numerical integration of C_{inv}.

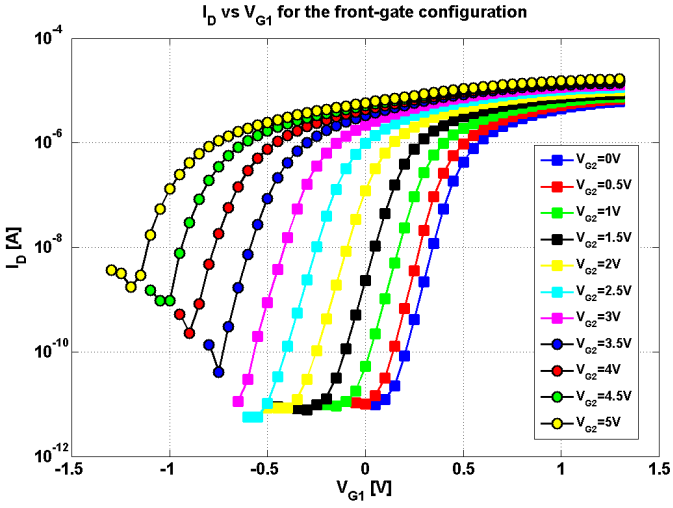

Figure 4: Drain current (I_D) vs. Front gate voltage (V_{G1}) for the front gate configuration. These parameters are directly extracted from the devices.

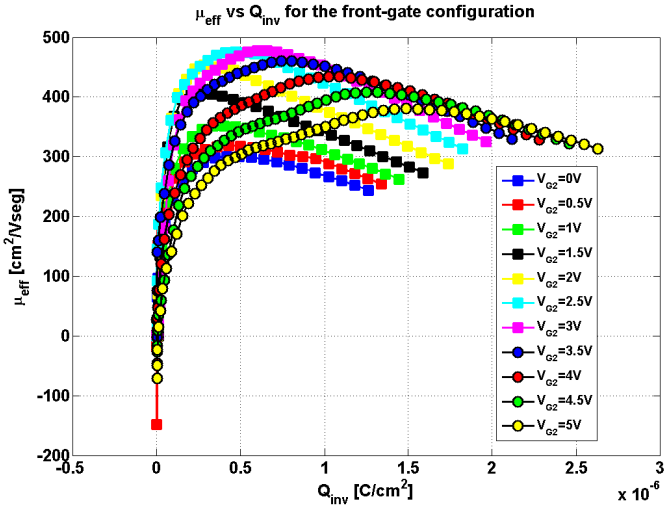

Figure 5: Mobility (μ_{eff}) vs Inversion charge ($\mathrm{Q_{inv}}$) for the front gate configuration. Equation (1) is used for the mobility computation.

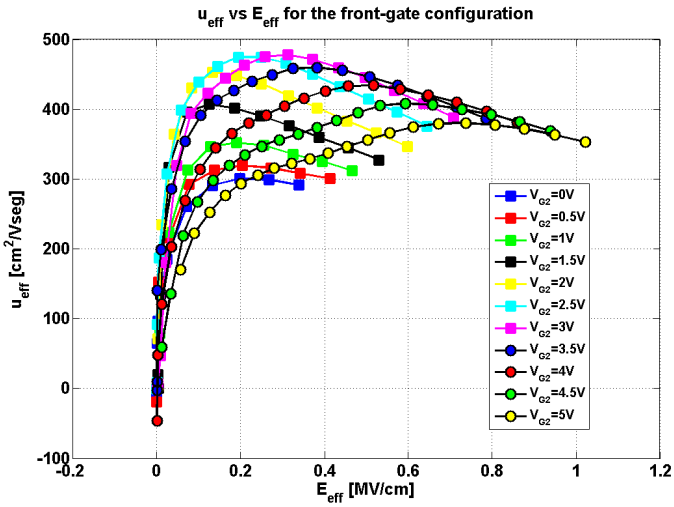

Figure 6: Mobility (μ_{eff}) vs Effective electric field ($\mathrm{E_{eff}}$) for the front gate configuration. Equation (2) is used for the electric field computation.

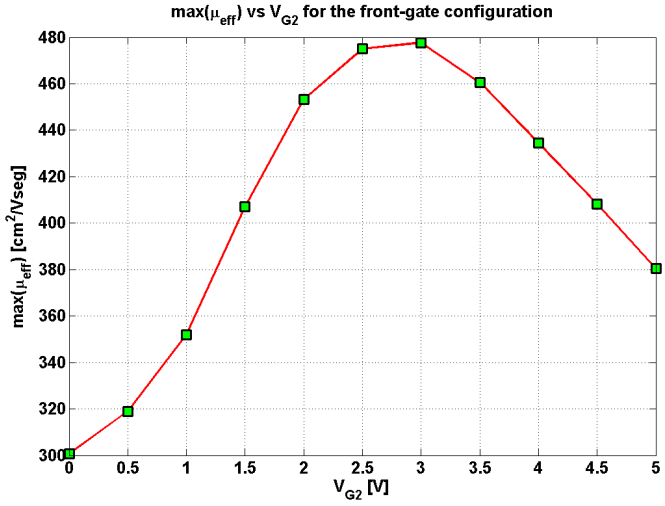

Figure 7: Mobility Peak ($\mathrm{max}(\mu_{\mathrm{eff}})$) vs. Back gate voltage ($\mathrm{V_{G2}}$) for the front gate configuration. Maximum electron transport occurs at $\mathrm{V_{G2}}$=3V.

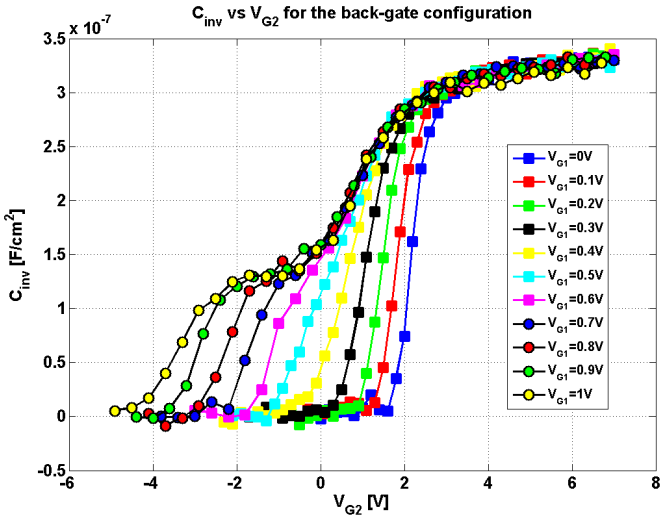

Figure 8: Inversion capacitance (C_{inv}) vs. back-gate voltage (V_{G2}) for the back-gate configuration. These parameters are directly extracted from the devices.

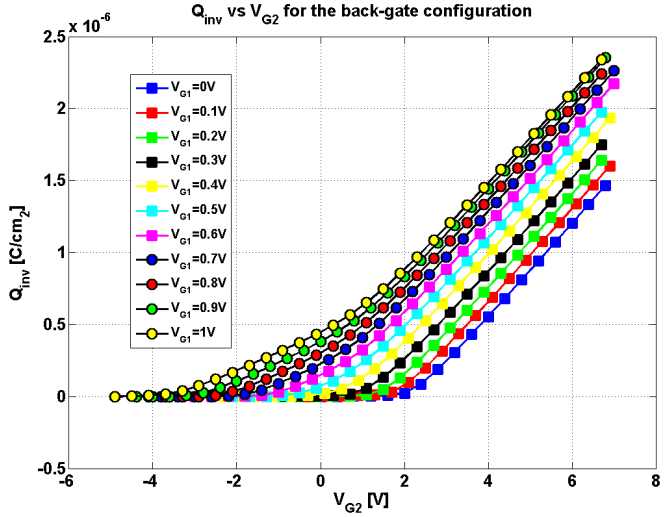

Figure 9: Inversion charge (Q_{inv}) vs. back-gate voltage (V_{G2}) for the back-gate configuration. These curves are the result of the numerical integration of C_{inv}.

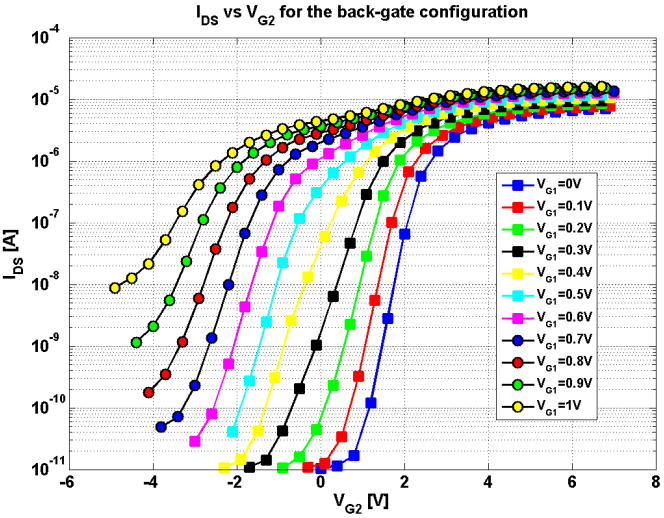

Figure 10: Drain current (I_D) vs. back-gate voltage (V_{G2}) for the back-gate configuration for the back-gate configuration.

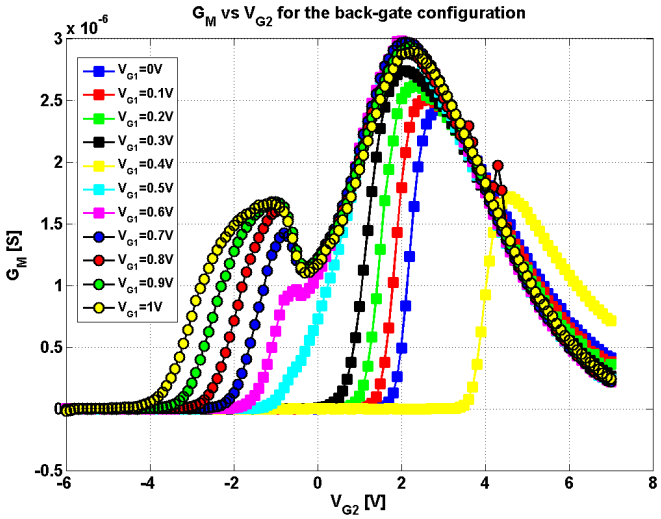

Figure 11: Trans-conductance (G_M) vs. back-gate voltage (V_{G2}) for the back-gate configuration for the back-gate configuration. Two peaks are evident for voltajes V_{G1}>0.5V.

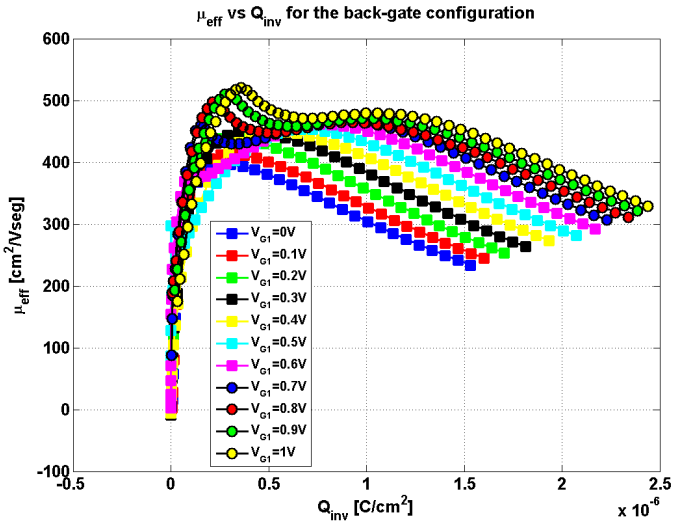

Figure 12: Mobility (μ_{eff}) vs Inversion charge (Q_{inv}) for the back-gate configuration. Equation (1) is used for the mobility computation. A second peak can be observed for V_{G1}>0.5V.

11. We can see that there are two local maxima for the curves V_{G1} $\geq$0.6V. The first peak is caused by the activation of the front gate and is lower than the second one.

Figures 12 and 13 show the curves μ_{eff} vs. Q_{inv} and μ_{eff} vs. E_{eff} for different V_{G1}. For curves V_{G1} $\geq$0.6V, we can see that there are two local maxima of mobility, as we obtained for G_M. In this case, the first peak is higher than the second one which is consistent with the low capacitive value of C_X. The nature of this peak is not clear and a further study is needed to determine its role. However, it occurs only for negative back-gate bias, corresponding to strongly decreasing front-gate mobility; which is our main interest in this work.

The peak of mobility vs. V_{G1} is shown in Figure 14. If we eliminate the first peak of mobility for curves V_{G1} $\geq$ 0.6V, we can see that the mobility stabilizes at V_{G1}=0.4V with μ_{eff}=450 cm^2/V.s. Again, the increase of the mobility peak with respect to V_{G1} is because of the activation of the front-channel. The contribution of the front-channel is able to increase the back-gate mobility in around 150%. The maximum values of mobility obtained in both configurations are very similar (6.66% of discrepancy) which confirms that the back-channel is the only one activated in the front-gate configuration consistent with [9].

Conclusions

The mobility parameter was extracted successfully in UTBB-FD-SOI-MOSFETs devices for the front and back-gate configurations. The maximum values of electron transport were obtained for V_{G2}=3V for the front gate configuration. A 60% of mobility increase can be obtained by the contribution of the back-gate, which increases the device performance considerably. In the case of the back-gate configuration, the tendency of the re-

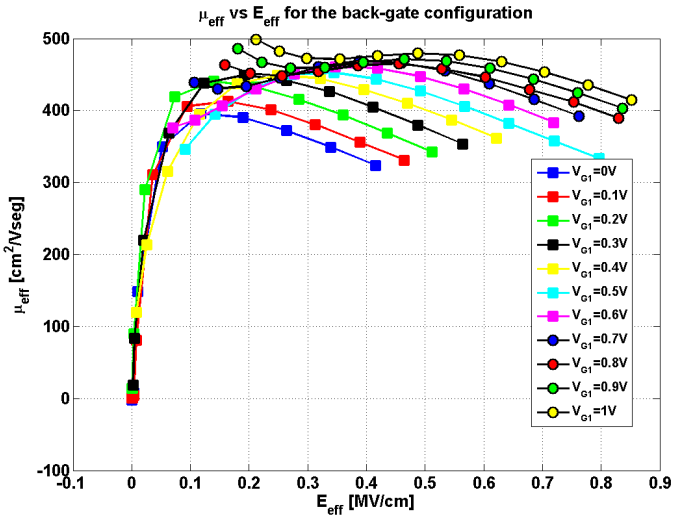

Figure 13: Mobility (μ_{eff}) vs Effective electric field ($\mathrm{E_{eff}}$) for the back-gate configuration. Equation (2) is used for the electric field computation, with the respective changes.

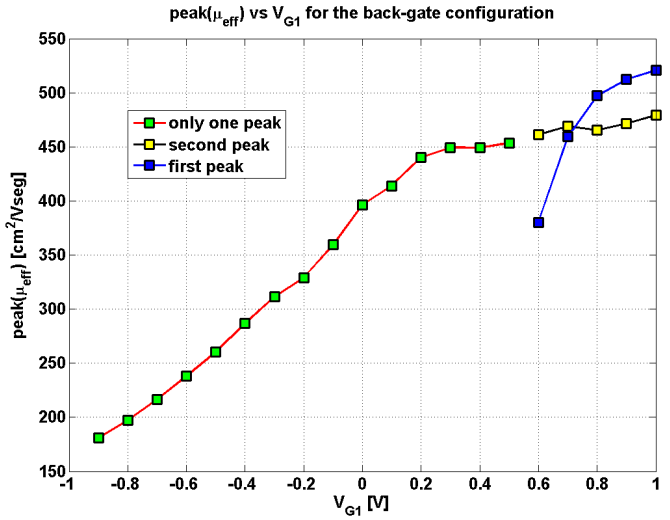

Figure 14: Mobility Peak ($\max(\mu_{\mathrm{eff}})$) vs. front-gate voltage ($\mathrm{V_{G1}}$) for the back-gate configuration. From $\mathrm{V_{G1}}$=06.V two mobility peaks can be observed. The first peak rises faster than the second, this is related with the first trans-conductance peak.

sults was different: two peaks were obtained for the curves of trans-conductance and mobility. The appearance of the first peaks, in both curves, is related with the activation of the front gate.

The presence of an additional capacitive component, C_x, causes a large increment of the first mobility peaks for the curves V_{G1} $\geq$0.6V, but this peak is related to the negative V_{G2} bias, where the front-gate mobility is getting decreased. Note that the maximum values of mobility stabilize at V_{G1}=0.4V. In the back-gate configuration, the contribution of the front-gate bias is able to increase the back-gate mobility in 150%. These experiments confirm that back-channel is the only one activated when the front channel reach its maximum. However, for larger V_{G2}, the mobility decreases in the front-gate configuration. In further experiments, it is planned to study the transport for *high-k* devices and understand what is happening for large V_{G2}.

Acknowledgments

The authors would like to thank Imec (Belgium) for providing the studied UTBB-FD-SOI-MOSFETs samples.

References

[1] Cristoloveanu, S. 2001. "Silicon on insulator tecnologhies and devices: from present to future". *Solid-State Electronics*, 83:1403.

[2] Cristoloveanu, S.; Ghibaudo, G.; Ouisse, T.; Horiguchi, S.; Ono, Y.; Takahashi, Y.; Murase, K. 2003. "Ultimately Thin Double-Gate SOI MOSFETs". *IEEE Transactions on Electron Devices*, 50:830.

[3] Ernst, T.; Tinella, C.; Raynaud, C.; Cristoloveanu, S. 2002. "Fringing fields in sub-0.1μm FD SOI MOSFETs: Optimization of the device architecture". *Solid State Electron.*, 46:373.

[4] Naveh, Y.; Likharev, K. 2000. "Modeling of 10-nm-scale ballistic MOSFETŠs". *IEEE Electron Device Letter*, 21: 242.

[5] AMD. 2013. "AMD FX Processor Model Number and Feature Comparison". *http://www.amd.com/us/products/desktop/processors/amdfx/Pages/amdfx-model-number-comparison.aspx*. Access date: April 19th, 2013.

[6] Ohata, A.; Cassé, M.; Cristoloveanu, S. 2007. "Front- and back-channel mobility in ultrathin SOI-MOSFETs by front-gate split CV method". *Solid State Electron.*, 51: 245.

[7] Esseni, D.; Sangiorgi, E. 2004. "Low field electron mobility in ultra-thin SOI MOSFETs: experimental characterization and theoretical investigation". *Solid State Electron.*, 48:927.

[8] Takagi, S.; Toriumi, A.; Iwase, M.; Tango, H. 1994. "On the Universality of Inversion Layer Mobility in Si MOSFET's: Part I-Effects of Substrate Impurity Concentration". *IEEE Transactions on Electron Devices*, 41:2357.

[9] Ohata, A.; Bae, Y.; Fenouillet-Beranger, C.; Cristoloveanu, S. 2012. "Mobility Enhancement by Back-Gate Biasing in Ultrathin SOI MOSFETs With Thin BOX". *IEEE Electron Devices Letters*, 33:348.